What is claimed is:

1. A method for multiplying the frame rate of an input video signal having a line rate $f_H$in and a frame rate $f_V$in, comprising the steps of:

propagating said input video signal through just enough memory to delay said input video signal by a fraction of a frame period $1/f_V$in;

speeding up said delayed video signal to a first line rate faster than $f_H$in;

speeding up said input video signal to said a second line rate faster than $f_H$in;

supplying said speeded up video signal and said delayed speeded up video signal sequentially, one line at a time; and,

writing said sequentially supplied lines into a liquid crystal display at said faster line rate,

thereby writing at least some of said lines multiple times within each said frame period.

2. The method of claim 1, comprising the steps of:

supplying a plurality of delayed output video signals; and,

speeding up each of said plurality of delayed video signals to said first and second faster line rates; and,

sequentially supplying all of said speeded up video signals for said writing step.

3. The method of claim 1, comprising the steps of:

periodically interrupting said supplying step to supply a number of consecutive lines of said speeded up video signal;

periodically interrupting said supplying step to supply a number of consecutive lines of said delayed speeded up video signal; and,

alternating said interrupting steps to maintain a uniform time interval between writing lines into the same line-number position on said liquid crystal display.

4. The method of claim 1, comprising the step of writing said lines to a liquid crystal on silicon display.

5. The method of claim 1, comprising the step of propagating said input video signal through a memory embedded in an integrated circuit.

6. The method of claim 1, comprising the step of propagating said input video signal through just enough memory to delay said input video signal by $(n-1)/n$ of said frame period, where n is a multiplication factor of said frame multiplying.

7. The method of claim 1, comprising the steps of:

at least doubling said frame rate of said input video signal; and,

writing each of said lines multiple times to said liquid crystal display.

8. The method of claim 1, comprising the step of speeding up said delayed video signal and said input video signal to the same line rate faster than $f_H in$.

9. A method for doubling the frame rate of an input video signal having a line rate $f_H in$ and a frame rate $f_V in$, comprising the steps of:

propagating said input video signal through just enough memory to delay said input video signal by $1/2$ of a frame period $1/f_V in$;

speeding up said delayed video signal to a first line rate faster than $f_H$in;

speeding up said input video signal to a second line rate faster than $f_H$in;

supplying said speeded up video signal and said delayed speeded up video signal sequentially, one line at a time; and,

writing said sequentially supplied lines into a liquid crystal display at said faster line rate,

thereby writing each of said lines twice within each said frame period.

10. The method of claim 9, comprising the steps of:

periodically interrupting said supplying step to supply a number of consecutive lines of said speeded up video signal;

periodically interrupting said supplying step to supply a number of consecutive lines of said delayed speeded up video signal; and,

alternating said interrupting steps to maintain a uniform time interval between writing lines into the same line-number position on said liquid crystal display.

11. The method of claim 9, comprising the step of writing said lines to a liquid crystal on silicon display.

12. The method of claim 9, comprising the step of propagating said input video signal through a memory embedded in an integrated circuit.

13. The method of claim 9, comprising the step of speeding up said delayed video signal and said input video signal to the same line rate of $2f_H$in.

14. A frame rate multiplier for an input video signal having a line rate $f_{H}in$ and a frame rate $f_{V}in$, said frame rate multiplier comprising:

a first memory for said input video signal, said first memory having a maximum required data storage capacity just large enough to delay said input video signal for a fraction of a frame period $1/f_{V}in$;

a second memory for speeding up said delayed video signal to a first line rate faster than $f_{H}in$;

a third memory for speeding up said input video signal to a second line rate faster than $f_{H}in$;

a multiplexer coupled for receiving both said speeded up video signals and supplying said speeded up video signals one line at a time for writing to a liquid crystal display, and,

a source of clock signals and control signals, said source being coupled to each of said memories, to said multiplexer and to said liquid crystal display, such that successive lines supplied by said multiplexer to said liquid crystal display originate alternately from said second and third memories at said faster line rates, at least some of said supplied lines being supplied to said liquid crystal display multiple times within each said frame period.

15. The frame rate multiplier of claim 14, wherein said maximum required data storage capacity of said first memory is $(n-1)/n$ of a frame, where n is the multiplication factor of said frame rate multiplier.

16. The frame rate multiplier of claim 15, wherein said first memory has n-1 outputs for supplying n-1 delayed output video signals, where $n \geq 2$.

17. The frame rate multiplier of claim 16, comprising:

n-1 memories coupled to said first memory and to said multiplexer for speeding up said n-1 delayed output video signals to said faster line rates; and,

said lines supplied by said multiplexer to said liquid crystal display originating sequentially from said third memory and said n-1 memories.

18. The frame rate multiplier of claim 14, wherein said source of clock signals and control signals provides an operating mode in which said multiplexer is controlled to:

periodically interrupt said supply of said lines to said liquid crystal display;

supply to said liquid crystal display during said periodic interruptions a number of successive lines from said second memory or a number of successive lines from said third memory; and,

alternately select said number of successive lines from said second or third memory in order to maintain a uniform time interval between writing lines into the same line-number position on said liquid crystal display.

18. The frame rate multiplier of claim 14, wherein said frame rate multiplier is at least partly formed integrally in an integrated circuit.

19. The frame rate multiplier of claim 18, wherein said first memory is formed integrally in an integrated circuit.

20. The frame rate multiplier of claim 14, wherein said first and second memories are functionally combined into a single memory to both delay and speed up said input video signal.

21. The frame rate multiplier of claim 14, wherein said first, second and third memories are functionally combined into a single memory to delay and speed up said delayed input video signal and to speed up said input video signal.

22. The frame rate multiplier of claim 14, wherein said first and second faster line rates are the same.

23. A frame rate doubler for an input video signal having a line rate $f_H$in and a frame rate $f_V$in, said frame rate doubler comprising:

a first memory for delaying said input video signal for $1/2$ of a frame period $1/f_V$in;

a second memory for speeding up said delayed video signal to a line rate faster than $f_H$in;

a third memory for speeding up said input video signal to a second line rate faster than $f_H$in;

a multiplexer coupled for receiving both said speeded up video signals and supplying said speeded up video signals one line at a time for writing to a liquid crystal display, and,

a source of clock signals and control signals, said source being coupled to each of said memories, to said multiplexer and to said liquid crystal display, such that successive lines supplied by said multiplexer to said liquid crystal display originate alternately from said second and third memories at said faster line rate, each of said supplied line being supplied to said liquid crystal display twice within each said frame period.

24. The frame rate doubler of claim 23, wherein said first memory has a maximum required data storage capacity of 1/2 of a frame.

25. The frame rate doubler of claim 23, wherein said source of clock signals and control signals provides an operating mode in which said multiplexer is controlled to:

periodically interrupt said supply of said lines to said liquid crystal display;

supply to said liquid crystal display during said periodic interruptions n successive lines from said second memory or n successive lines from said third memory; and,

alternately select said n successive lines from said second or third memory in order to maintain a uniform time interval between writing lines into the same line-number position on said liquid crystal display.

26. The frame rate doubler of claim 23, wherein said liquid crystal display comprises liquid crystal on silicon.

27. The frame rate doubler of claim 23, wherein said frame rate doubler is at least partly formed integrally in an integrated circuit.

28. The frame rate doubler of claim 27, wherein said first memory is formed integrally in said integrated circuit.

29. The frame rate doubler of claim 23, wherein said first and second memories are functionally combined into a single memory to both delay and speed up said input video signal.

30. The frame rate multiplier of claim 23, wherein said first, second and third memories are functionally combined into a single memory to delay and speed up said delayed input video signal and to speed up said input video signal.

B' cancel

31. The frame rate multiplier of claim 23, wherein said first and second faster line rates are the same.